

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S16	3227	(438/3,240,486).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/09 11:23

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	232	"ferroelectric capacitor" and "ferroelectric capacitor" and "FeRam memory"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:05
L6	188	5 and ((@ad<"20030926") or(@rlad<"20030926"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/27 13:06

US-PAT-NO: 6384440

DOCUMENT-IDENTIFIER: US 6384440 B1

TITLE: Ferroelectric memory including **ferroelectric capacitor**,
one of whose electrodes is connected to metal silicide
film

----- KWIC -----

Application Filing Date - AD (1):
20001102

TITLE - TI (1):

Ferroelectric memory including **ferroelectric capacitor**, one of whose
electrodes is connected to metal silicide film

Brief Summary Text - BSTX (3):

The present invention relates to a ferroelectric memory. More particularly,
the present invention relates to a ferroelectric memory including a
ferroelectric capacitor used for a cell of the ferroelectric memory.

Brief Summary Text - BSTX (9):

FIG. 1 shows the structure of the known FeRAM. The known FeRAM employs a
planar type cell. The FeRAM is composed of a semiconductor substrate 501, a
ferroelectric capacitor 502 provided above the semiconductor substrate 501, and
a protecting film 503 of SiO.sub.2 provided on the ferroelectric capacitance
element 502.

Brief Summary Text - BSTX (10):

The **ferroelectric capacitor** 502 is composed of a lower electrode 504, an
upper electrode 505 and a ferroelectric film 506 that is sandwiched by them.
The upper electrode 505 is composed of IrO.sub.2 or Ir film.

Brief Summary Text - BSTX (13):

The **ferroelectric capacitor** 502 and the diffusion layer 509 are electrically
connected to a wiring layer 510 through the contact holes 507 and 508,
respectively.

Brief Summary Text - BSTX (26):

In the **ferroelectric capacitor**, it is possible to suppress the deterioration of the ferroelectric film resulting from an annealing process carried out after the formation of the metal wiring. This is because the metal silicide film is formed above the ferroelectric film. The metal silicide film effectively protects the bad influence on the ferroelectric film caused by the thermal stress of the wiring. As a result, the deterioration of the ferroelectric film is not easily induced. Moreover, in the **ferroelectric capacitor** according to the present invention, it is possible to protect the strip of the films of the wiring and the lower electrode and also avoid the conductive defect in a contact to the lower electrode and the increase in resistance. This is because the lower electrode and the metal silicide are not in direct contact with each other.

Brief Summary Text - BSTX (36):

In order to achieve another aspect of the present invention, a method of fabricating a ferroelectric memory is composed of forming a **ferroelectric capacitor** including:

Brief Summary Text - BSTX (43):

forming an interlayer insulating film on the **ferroelectric capacitor**;

Detailed Description Text - DETX (4):

FIG. 2 is a plan layout view showing an FeRAM of the first embodiment. The **FeRAM is provided with a memory** cell area 101 and a contact formation area 102. The memory cell area 101 is an area in which a memory cell of the FeRAM is formed. The contact formation area 102 is an area in which a contact between a wiring 17 and a lower electrode 9 serving as a plate line of the memory cell is formed.

Detailed Description Text - DETX (103):

Next, a titanium film having a thickness of 30 nm, a titanium nitride film having a thickness of 100 nm, an aluminum film having a thickness of about 500 nm and a titanium nitride film having a thickness of about 30 nm are deposited in turn. Then, those films and the metal silicide layer 23 are patterned to thereby form a metal wiring 17b connected to a bottom electrode 10 and a metal wiring 15. The **FeRAM memory** cell is formed by the above-mentioned processes.